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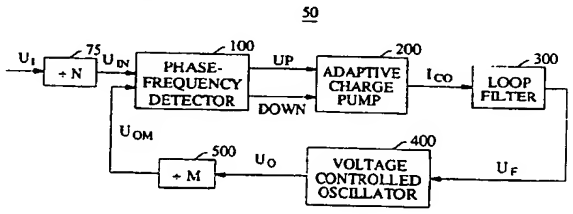
(54) Adaptive charge pump for phase-locked loops.

(57) A method and apparatus for improving the performance of a phase-locked loop (50) are disclosed. A phase error between two signals (U_{IN}, U_{OM}) is sensed (in 100) and a temporary increase in the band width of the phase-locked loop is provided responsive to the sensed phase error. The phase-locked loop may comprise a charge pump (200) and the temporary increase in the bandwidth of the phase-locked loop may comprise a temporary increase in charge pump current. An increase in phase-locked loop band-width is followed by a decrease in the bandwidth responsive to a decrease in phase error. The decrease in bandwidth may comprise a decrease in charge pump current.

FIG. 1



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of ordinary skill in the art that current sources controlled by switches in the VCS 260 and the VS 220 may comprise separate switches and sources, as presented in Figures 3 and 4, or unified switched current sources. Whether separate or together as a single element, such may be formed with field effect transistors using techniques well known in the art.

Operation of the Illustrative Embodiment

Under steady-state (*e.g.*, locked) conditions, the UP/DOWN logic signals from PFD 10 are infrequent and of short duration, if present at all. As a result, the duty cycle, DS, of signal S_1 from OR gate 225 is very small or zero (e.g., less than 10 percent). Switch 229 will therefore remain open most of the time and current source 227 will be largely blocked. (Under steady-state conditions, some conventional PFDs provide narrow UP/DOWN spikes from time to time; as will be appreciated by the ordinary artisan, these spies will not affect the fundamental operation of this embodiment.) At the same time, current source 233 is working to pull charge from capacitor 231 via resistor 235 at a rate of $I_2 = I_1/n$. Since $12 > I_1 \times DS$, the voltage across the capacitor, U_{VS}, is driven toward zero. The condition of $U_{VS} \leqq V_{th}$ is sensed by the threshold logic of inverter 237, causing it to output a logical TRUE signal. In response, inverter 239 provides a logical FALSE signal, U'_{VS}, to switches 285 and 287 of VCS 260. This FALSE signal causes the switches to open (or allows them to remain open). VCS 260 output current, I_{CO}, is therefore equal to I3, as provided by current source 265 or 275, when switch 290 or 292, respectively, is closed.

As a result of significant variations in the reference signal U_I, or in the programmable values of M and N (*e.g.*, resulting in loss of lock), significant UP-/DOWN logic pulse signals are produced. Accordingly, the duty cycle, DS, of signal S_1 is large (*e.g.*, greater than 10 percent). Switch 229 will close whenever signal S_1 is TRUE. Each time switch 229 closes, current I_1 is allowed to flow and, as a result, charge is deposited on capacitor 231. If the current $I_1 \times DS$ (the rate at which charge is being deposited on the capacitor) exceeds the current 12 (the rate at which charge is being drained from the capacitor), the voltage at node B, U_{VS}, will be driven toward the supply voltage, V_{DD}. The condition of $U_{VS} > V_{th}$ is sensed by the threshold logic of inverter 237, causing inverter 237 to output a logical FALSE signal. In response, inverter 239 provides a logical TRUE signal, U'_{VS}, to switches 285 and 287 which close in response. During the time when switches 285 and 287 are closed and UP-/DOWN pulses are present, VCS 260 output current, I_{CO}, is equal to I3, as provided by current source 265 or 275, *plus* I_4, as provided by current source 270 or 280. Responsive to increased output current, I_{CO}, the bandwidth of the PLL 50 is increased thus enhancing its variation settling properties.

As a result of the VCO 400 adjusting its output signal to reduce the PLL 50 phase error (between signal U_{IN} and output signal U_{OM}) to a small, if not zero, level, the PFD 100 will cease generating significant UP/DOWN logic pulses. Absent such significant logic pulses, the voltage at node B of the VCS 260, U_{VS}, is driven toward zero by current source 233. The condition of $U_{VS} \leqq V_{th}$ is sensed by the threshold logic of inverter 237 causing it to provide a logical TRUE signal as output. This signal is inverted by inverter 239 to a logical FALSE signal causing switches 285 and 287 to open. As a result, VCS 260 may provide output current equal to I_3 from sources 265 and 275, depending on the presence of UP/DOWN logic pulses at switches 290 and 292, respectively. Responsive to this level of output current, the PLL 50 exhibits a reduced level of phase jitter compared with that exhibited by the PLL 50 when its output current equals the sum of I_3 and I_4.

Claims

1. In a phase-locked loop including a loop filter, an oscillator providing an output signal of the phase-locked loop, a phase detector, and a charge pump providing current to the loop filter, the current having a magnitude, a method of adjusting the bandwidth of the phase-locked loop, the method comprising the steps of:

   the phase detector sensing a phase error between a reference signal and the output signal of the phase-locked loop;

   the charge pump increasing the magnitude of the current provided to the loop filter responsive to the phase error sensed by the phase detector, and

   subsequent to increasing the magnitude of the current, the charge pump decreasing the magnitude of the current.

2. The method of claim 1 wherein the charge pump increases and decreases the magnitude of the current by the same amount.

3. The method of claim 1 wherein the step of the charge pump decreasing the magnitude of the current is performed in response to a decrease in sensed phase error by the phase detector.

4. In a phase-locked loop including a loop filter, an oscillator, and a phase detector for detecting errors between a reference signal and an output signal of the loop, an adaptive charge pump for coupling to the phase detector and the loop filter in the phase-locked loop and for providing charge pump current to the loop filter, the charge pump

current having a magnitude, the adaptive charge pump comprising:

a. a variation sensor for determining when the magnitude of charge pump current provided to the loop filter should be increased, the determination to increase the magnitude of charge pump current based upon a phase error detected by the phase detector, and

b. a variable current source, coupled with the variation sensor, for providing charge pump current to the loop filter and for providing

1. an increase in the magnitude of charge pump current responsive to said determination by the variation sensor, and

2. subsequent to providing said increase, a decrease in the magnitude of charge pump current.

5. The adaptive charge pump of claim 4 wherein the increase and decrease in the magnitude of charge pump current are equal.

6. The adaptive charge pump of claim 4 wherein the variable current source provides a decrease in the magnitude of charge pump current responsive to a decrease in phase error detected by the phase detector.

7. The adaptive charge pump of claim 4 wherein the variation sensor comprises:

a capacitor,

first current source means for producing a first current for use in charging the capacitor, said first current being provided responsive to a phase error detected by said phase detector,

second current source means for producing a second current for use in discharging the capacitor, and

means for determining when the magnitude of charge pump current should be increased responsive to a voltage across the capacitor.

8. The adaptive charge pump of claim 7 wherein the magnitude of the first current is substantially ten times the magnitude of the second current.

9. A phase-locked loop comprising:

a. a phase detector for sensing a phase error between a reference signal and an output signal of the phase-locked loop;

b. a loop filter, the loop filter for receiving a current having a magnitude and for providing a filter output signal;

c. a variation sensor for determining when the magnitude of current received by the loop filter should be increased, the determination to increase the magnitude of current based on a phase error sensed by the phase detector;

d. a variable current source for providing current to the loop filter, and for providing

1. an increase in the magnitude of said current responsive to said determination by the variation sensor, and

2. subsequent to providing said increase, a decrease in the magnitude of said current; and

e. an oscillator for providing the phase-locked loop output signal responsive to the filter output signal.

10. The phase-locked loop of claim 9 wherein the increase and decrease in the magnitude of said current are equal.

11. The phase-locked loop of claim 9 wherein the variable current source provides a decrease in the magnitude of said current responsive to a decrease in phase error detected by the phase detector.

12. The phase-locked loop of claim 9 further comprising a divider circuit, coupled between the phase detector and the oscillator, for dividing the frequency of the phase-locked loop output signal by a predetermined number.

13. The phase-locked loop of claim 12 filter comprising a reference signal divider circuit, coupled to the phase detector, for dividing the frequency of the reference signal by a predetermined number.

14. The phase-locked loop of claim 13 wherein each of the divider circuits is independently programmable to allow selection of the predetermined numbers.

15. The phase-locked loop of claim 9 wherein the phase detector comprises a phase-frequency detector.

FIG. 1

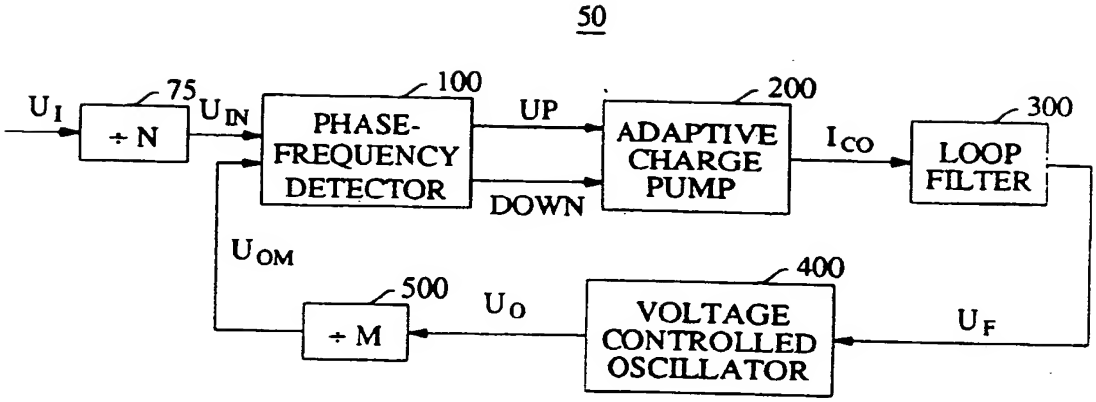


FIG. 2

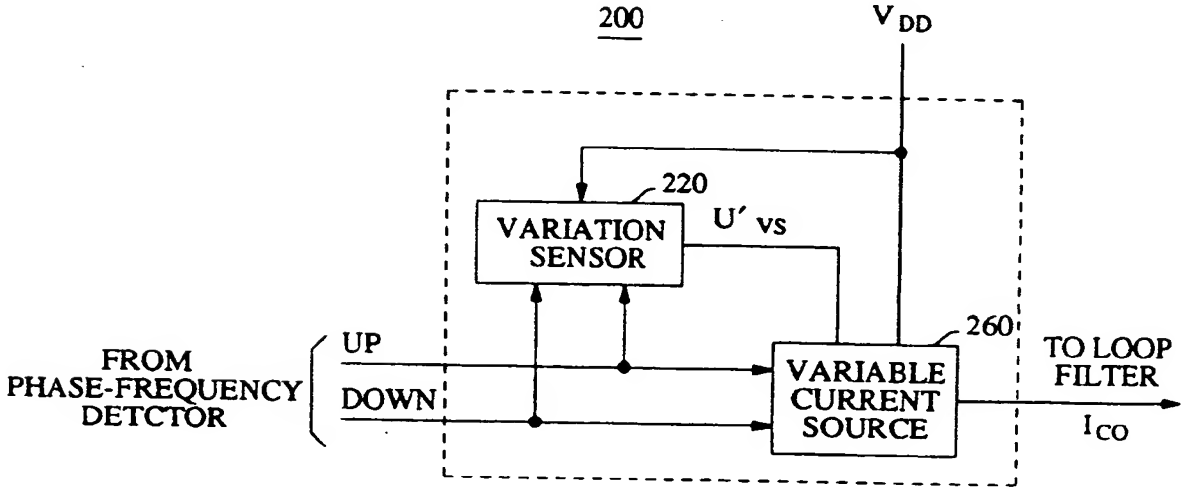


FIG. 3

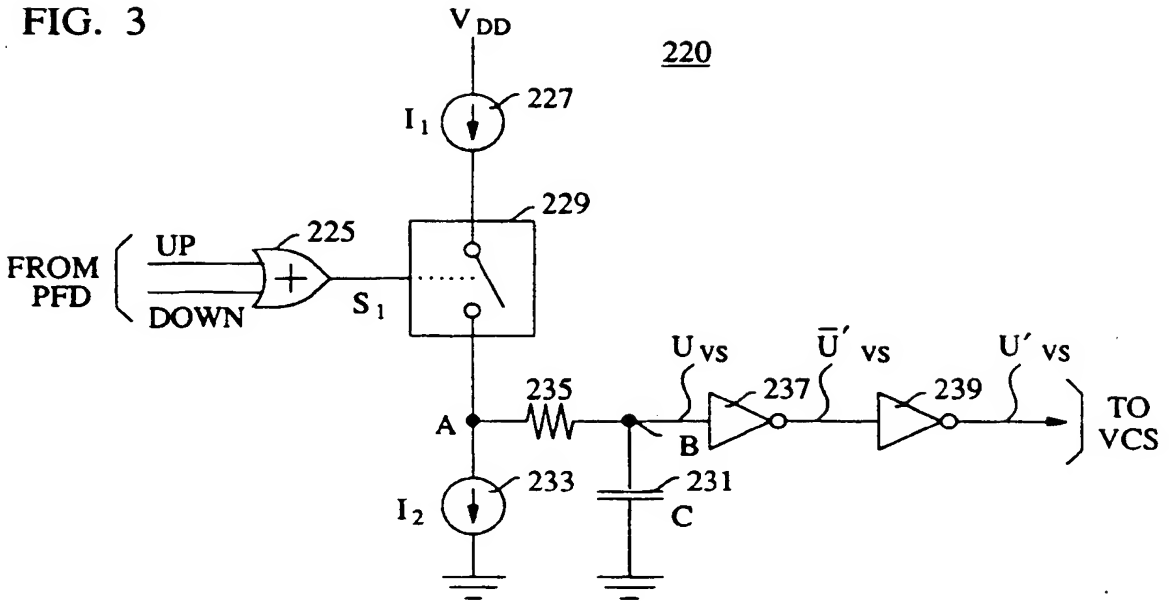
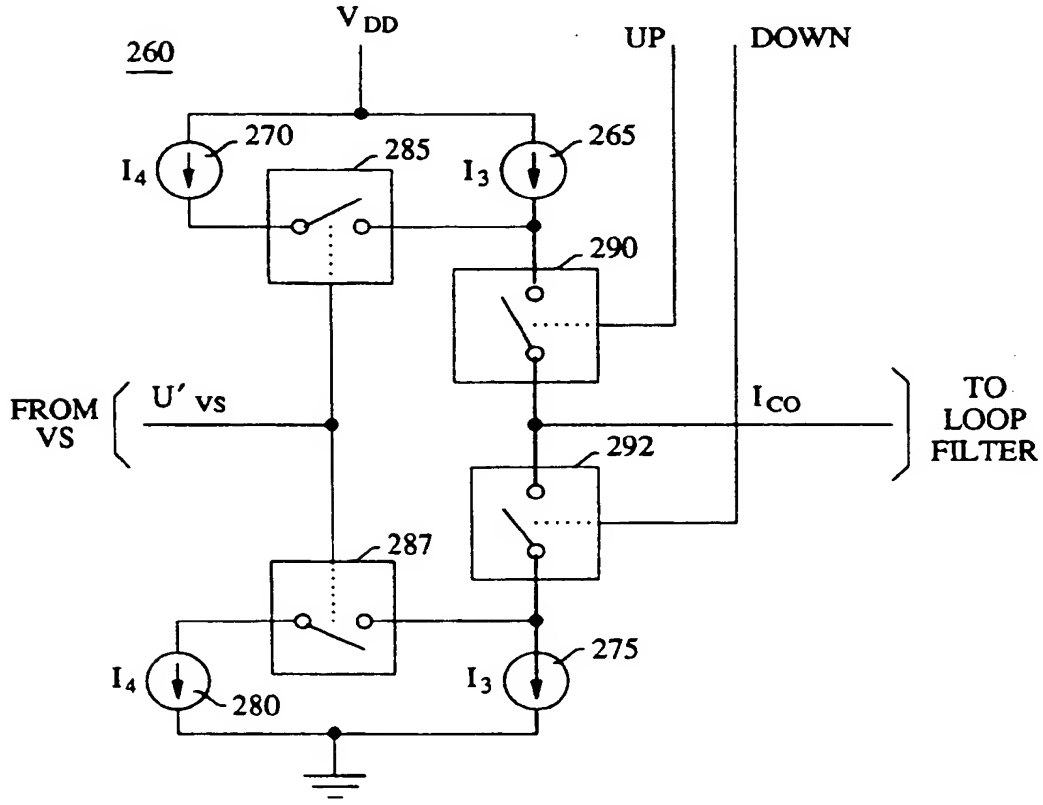


FIG. 4



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EUROPEAN SEARCH REPORT

Application Number
EP 92 30 7433

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	US-A-4 745 372 (MIWA) * column 1, line 41 - line 43 * * column 3, line 8 - column 6, line 6; figures 2-5,7-9 *	1-15	H03L7/107
A	US-A-4 122 405 (TIETZ ET AL.) * column 2, line 17 - column 3, line 68; figure *	7,8	
X	US-A-4 156 855 (CROWLEY) * column 1, line 25 - column 4, line 28; figures *	1-6, 9-11,15	
X	US-A-4 926 141 (HEROLD ET AL.) * column 3, line 46 - column 12, line 21; figures *	1-6,9-15	
P,X	EP-A-0 458 269 (NEC CORPORATION) * column 2, line 57 - column 5, line 16; figure 3 *	1-6, 9-12,15	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H03L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	23 JULY 1993	BALBINOT H.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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E : earlier patent document, but published on, or after the filing date
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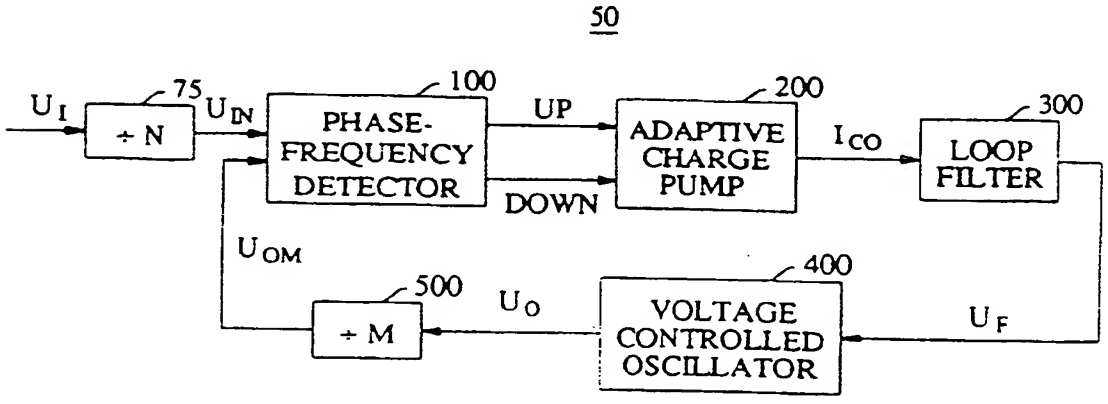

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